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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/698,093	10/31/2003	Henry Wurzburg	5707-05300	1009

7590 11/01/2005

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EXAMINER	
DOAN, DUC T	

ART UNIT	PAPER NUMBER
2188	

DATE MAILED: 11/01/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/698,093	WURZBURG, HENRY	
	Examiner	Art Unit	
	Duc T. Doan	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 June 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-43* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-43* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *6/1/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Status of Claims

Claims 1-43 are in the application.

Claims 1-43 are rejected.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

A person shall be entitled to a patent unless -

(a) the invention was known or used by other's in this country or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in a patent granted on an application for patent by another fled in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

Claims 1-2,4,10-12,16-18,24-35,38-43 rejected under 35 U.S.C. 102 (e) as being anticipated by Piau (US Pub 2004/0049627); (evidentiary reference: Blood et al (US Pub 2003/0110351)).

As for claim 1, Piau describes a flash-memory card-reader system comprising: a hard disk controller interface (Fig 2: # 204 IDE interface); a buffer coupled to the hard disk controller interface (Fig 2: #214); a processing unit coupled to the buffer (Fig 2: #216); and a flash-memory card-controller unit coupled to the buffer and to the processing unit (Fig 2: #220); wherein the hard disk controller interface is operable to communicate with a hard disk controller in a host system (Piau's page 2, paragraph 18) , wherein the hard disk controller interface is operable to receive incoming commands from the hard disk controller (Piau's page 2, paragraph 18); and wherein the processing unit is operable to translate the incoming commands to produce translated incoming commands usable by the flash-memory card-controller unit, wherein the processing unit is operable to provide the translated incoming commands to the flash-memory card-controller unit (Piau's pages 3,4 paragraph 29,30 describes converting original command into read write command of flash data blocks).

As for claim 2, Piau's wherein the hard disk controller comprises and IDE/ATA controller; and wherein the incoming commands are ATA commands (Fig 2: #203).

As for claim 4, Piau describes wherein the flash-memory card-controller unit is operable to access a flash memory card in response to the translated incoming commands (Piau's pages 3,4 paragraph 29,30 describes converting original command into read write command of flash data blocks).

As for claim 10, Piau describes wherein the flash-memory card-reader system appears as a HDD to the host system (Piau's Fig 2: #203,204 page 2 paragraph 20 describes the flash memory controller provides various disk drive interfaces such as ATA, IDE to communicate with host in both directions).

As for claim 11,the claim recites wherein the processing unit is operable to: translate outgoing commands issued by the flash-memory card-controller unit to produce translated outgoing commands; and provide the translated outgoing commands to the hard disk controller interface; and wherein the hard disk controller interface is operable to receive the translated outgoing commands and provide the translated outgoing commands to the hard disk controller in the host system. (Piau's Fig 2: #203,204 page 2 paragraph 20 describes the flash memory controller provides various disk drive interfaces such as ATA, IDE to communicate with host in both directions; pages 2,3 paragraph 22 describes the flash memory controller gathering configuration structures information and provide this information to the host using commands of interfaces such as ATA, IDE.

As for claim 12, the claim recites wherein the translated outgoing commands comprise ATA commands. The claim rejected base on the same rationale as in the rejection of claim 11.

Claims 16,28,31,38 rejected based on the same rationale as in the rejection of claim 1.

Claims 17,32 rejected based on the same rationale as in the rejection of claim 2.

Claim 18 rejected based on the same rationale as in the rejection of claim 4.

Claim 20 rejected based on the same rationale as in the rejection of claim 6.

Claims 24,29 rejected based on the same rationale as in the rejection of claim 10.

Claims 25,30 rejected based on the same rationale as in the rejection of claim 11.

Claims 26,39 rejected based on the same rationale as in the rejection of claim 12.

As for claims 33-35, the claims recite wherein a microprocessor coupled to the IDE controller (claim 33); wherein the microprocessor comprises an embedded microprocessor (claim 34); wherein the system comprises an embedded system (claim 35). Although Piau does not

mention the embedded aspect of the claim. It has been known in the art that an embedded system with embedded processors and embedded disk controller devices are packaging together for example in a motherboard or backplane of a system. This teaching is evident in Blood et al (US Pub 2003/0110351, page 2, paragraphs 17-19), which is introduced here as an evidentiary reference.

As for claim 40, the claim rejected based on the same rationale as in the rejection of claim 33.

As for claims 41-42, wherein the outgoing commands issued by the flash-memory card-controller are in response to the translated incoming commands (claim 41); transferring data from the flash-memory card to a host system that comprises the IDE controller; wherein said accessing comprises obtaining the data from the flash-memory card; and wherein said transferring is performed in conjunction with said providing the translated outgoing commands to the IDE controller (claim 42). The claims rejected based on the same rationale as in the rejection of claims 1-2. Day further describes the control circuits translating and transferring commands, status, data in both directions as shown in Fig 1, 2,3.

As for claim 43, the claim rejected base don the same rationale as in the rejection of claim 1. Piau's page 2 paragraph 21 describes the controller translate to compact flash command sequences to write and read, powering up, initializing flash memory devices.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 3,13-15 rejected under 35 U.S.C. 103(a) as being unpatentable over Piau (US Pub 2004/0049627) as applied to claim 1, and further in view of Day et al (US Pub 2004/0019734).

As for claim 3, the claim recites wherein the hard disk controller comprises a SCSI controller; and wherein the incoming commands are SCSI commands. Piau does not describe the hard disk controller with SCSI interface. However, Day describes an integrated circuit with SCSI interface and capable of translating SCSI commands and protocol into ATA protocol (Fig 1: #110). It would have been obvious to one of ordinary skill in the art at the time of invention to include protocol translating circuits as suggested by Day in Piau's system to translate SCSI protocol into ATA protocol thereby allowing users to maintain existing SCSI software structures while utilizing cost efficient ATA storage devices (Day's page 1 paragraph 2, page 19 paragraph 19).

As for claim 13, the claim recites wherein the translated outgoing commands comprise SCSI commands. The claim rejected base on the same rationale as in the rejection of claim 11.

As for claim 14, the claim recites an ATA register emulation unit coupled between the buffer and the processing unit, wherein the ATA register emulation unit is configured to store

ATA command and status register information (Day's figures 2 describes ATA task file registers for command, data, status).

As for claim 15, the claim recites a SCSI register emulation unit coupled between the buffer and the processing unit, wherein the SCSI register emulation unit is configured to store SCSI command and status register information (Day's figures 4 describes SCSI commands being stored and convert to corresponding ATA command).

Claims 5-9,19-23,36-37 rejected under 35 U.S.C. 103(a) as being unpatentable over Piau (US Pub 2004/0049627), Day et al (US Pub 2004/0019734) and further in view of Tsao (US Pub2005/0029348).

As for claims 5-7, the claims recite a housing comprising at least one slot for receiving a flash-memory card; wherein the flash-memory card-controller unit is coupled to the housing; wherein the flash-memory card-controller unit is operable to access the flash-memory card in response to the translated incoming commands (claim 5); wherein the hard disk controller interface, the buffer, the processing unit, and the flash-memory card-controller unit are comprised in the housing (claim 6); wherein the flash-memory card comprises one of a Compact Flash Card, a Secure Digital Card, a Multi Media Card, a Smart Media Card, and a Memory Stick Card (claim 7). Piau describe a device located between host and flash memory modules with capability of translating host's commands. Piau does not describe the claim's aspect of the housing for the device. However, housing of a memory card with multiple slots for different type of memory card devices and an interface to the host has been known in the art. This teaching is evident in Tsao (US 2005/00293348, Fig 2, paragraph 15), which is introduced here as an

evidentiary reference. It would have been obvious to one of ordinary skill in the art at the time the invention was made to integrate the housing as suggested by Tsao to the system of Piau to allow connecting multiple memory devices into multiple slots of the housing thereby readily providing a single package for communicating different memory devices to a host (Tsao's paragraph 4).

As for claim 8, the claim recites a housing comprising one or more slots, wherein each respective one of the one or more slots is configured to receive a respective flash-memory card; wherein the respective flash-memory card comprises one of the following types: Compact Flash; Secure Digital; Multi Media; Smart Media; and Memory Stick; and wherein the flash-memory card-controller unit is operable to access the respective flash-memory card in response to the translated incoming commands. The claim rejected based on the same rationale as in the rejection of claims 5-7.

Claim 9 rejected based on the same rationale as in the rejection of claim 8.

Claim 19 rejected based on the same rationale as in the rejection of claim 5.

Claim 21 rejected based on the same rationale as in the rejection of claim 7.

Claim 27 rejected based on the same rationale as in the rejection of claim 14.

Claims 22,36 rejected based on the same rationale as in the rejection of claim 8.

Claims 23,37 rejected based on the same rationale as in the rejection of claim 9.

Conclusion

When responding to the office action, Applicant is advised to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist examiner to locate the appropriate paragraphs.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Duc T. Doan whose telephone number is 571-272-4171. The examiner can normally be reached on M-F 8:00 AM 05:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on 571-272-4210. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Kevin L. Ellis
Primary Examiner